REMARKS

In response to the Office Action mailed February 4, 1997, Applicant respectfully requests reconsideration. The drawings were objected to because of informalities. Claims 3 and 13 were objected to because of informalities. Claims 1-4, 6-11, 13-14, 16-22, and 24-25 were rejected under 35 U.S.C. § 112, first paragraph, as not being enabled by the specification. Claim 25 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1-4, 6-11, 13-14, 16-19, 21 and 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Matsumura. Claims 1-4, 6-11, 13-14, 16-19, 21, and 24 were rejected under 35 U.S.C. § 102(b) as anticipated by or under 35 U.S.C. § 103 as obvious over Okada. Claims 20, 22, and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumura. Claims 20, 22 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Okada. Applicants have amended the claims and proposed amendments to the drawings. The application is now in condition for allowance.

Applicants wish to thank the examiner for the courtesy shown during the telephone interview of April 24, 1997 with applicants' attorney. During that interview, the objection to the drawings and rejection of the claims under 35 U.S.C. § 112, first paragraph, as not being enabled were discussed. In the office action, the drawings were objected to and the claims rejected allegedly because the diodes represented in FIGS. 3 and 5 have the wrong polarities. In response to a similar objection and rejection in the prior office action, applicants had responded that the drawings were correct. It appears that applicants and the examiner had different understandings of the meanings of the

representation of the bulk diodes in FIGS. 3 and 5. In the present office action, the examiner has referred to Kopera as a representation of the parasitic or bulk diode of a transistor. In Kopera, the diode is connected between the source and drain of the transistor. In the amendment filed May 13, 1996, applicants included a drawing indicating the understanding of the parasitic diodes represented in FIGS. 3 and 5. Clearly, the representation in FIGS. 3 and 5 had the same meaning as the different representation which was used by Kopera. In order to expedite prosecution of this application, applicants have proposed amendments to the drawings to redraw the parasitic diodes using the same representation as Kopera. This proposed change was discussed with the examiner in the telephone interview. No new matter is added by this change since it merely changes a representation of the parasitic diodes, which are a known part of the transistors. The description in the specification of the operation of the device has not changed and remains correct. Accordingly, approval of the changes is respectfully requested. The revisions also overcome the objections to the drawings and the rejections to the claims under 35 U.S.C. § 112, first paragraph.

Claim 25 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The language noted in the office action has been changed. Accordingly, the rejected under 35 U.S.C. § 112, second paragraph, has been overcome and should be withdrawn.

All of the claims were rejected as being anticipated by or obvious in view of two separate references, Matsumura and Okada. Applicants respectfully suggest that the present claimed invention distinguishes over the cited art. Both Matsumura and Okada relate to substrate bias generators, and, in the relevant portions of the circuits, are similarly connected. The structure is best

illustrated in FIG. 2A of Okada. There are two capacitors C1, C2, acting as inputs to the bias generator. The capacitors are connected on one side to complementary signals from an oscillator. The other side of the capacitors are connected to a voltage source V_{BB} through 2 MOS diodes TD1, TD2. The MOS diodes are P-channel transistors having their gates connected to the drain. Two P-channeled transistors connect the second side of the capacitors to the output V_{SS}. The gates of these two transistors are cross-connected to the second side of the other capacitor, thus, the transistors alternate to alternately charge the capacitor C1, C2 and then discharge them to the output V_{SS}.

The cited art does not teach or suggest the present invention. In the present application, a structure is disclosed which includes two P-type MOS transistors and two N-type MOS transistors. The different types of transistors allows all of the transistors to operate as switches, and allows the circuit to have a high efficiency. Also, the connections between the transistors operates to form two bridges, one with the conduction paths of the transistors and one with the bulk diodes of the transistors. The structures shown in Matsumura and Okada do not include the same connections so that two bridges are not formed. Thus, Matsumura and Okada have a significantly reduced efficiency over the structure of the present invention. The distinctions between the present invention and the cited art as set forth in the claims is discussed below.

Claim 1 recites a voltage doubler including an oscillator, a charge accumulation condenser, first and second charge transfer condensers, and a flip-flop structure. The flip-flop structure includes two inverters connected together in a loop to form the flip-flop. The structure has first and second inputs connected to the first and second charge transfer condensers, the negative power terminals are

connected to a power voltage, and the positive power terminals are connected to the charge accumulation condenser. The flip-flop structure is not taught or suggested by the cited art as suggested in the office action. The office action suggests that transistors T1, TD1 operate as an inverter because when P1 is high, P2 is low. However, P2 is not the output of an inverter including transistors T1, TD1. Rather, the output is V_{ss}. Similarly, in Matsumura, transistors 13, 15 and 14, 16 do not form two inverters. P1 and Q1 are not respective inputs and outputs of inverters, as suggested in the office action. Accordingly, the cited art does not teach or suggest two inverters connected together in a loop to form a flip-flop as recited in claim 1.

Furthermore, applicants have amended claim 1 to recite that the inverters are CMOS inverters. The CMOS inverter is a known structure including an N-channel transistor and a P-channel transistor. Both Matsumura and Okada only disclose P-channel transistors. There is nothing in the cited art which teaches or suggests the use of two different types of transistors in an inverter structure as part of a voltage doubler.

Therefore, for the reasons discussed above, claim 1 patentably distinguishes over the cited art and is in condition for allowance. Claim 2 depends from claim 1 and is allowable for at least the same reasons.

Claim 3 also relates to a voltage doubler including an oscillator, a charge accumulation condensor, first and second charge transfer condensors, and a structure. As recited in claim 3, the structure includes a bridge of four transistors and corresponding bulk diodes. As recited in claim 3, the four transistors and corresponding bulk diodes are arranged in order to have a certain set of

conduction path. First, the four transistors are arranged to have principal conduction paths in parallel with the four diodes. The control terminals of the transistors are connected to the first and second charge transfer condensors so as to lower a voltage drop along the branches of the bridge when the doubler reaches a steady state. As discussed int he specification, with the structure of the present invention, during a transient state, the diodes are conducting to generate an increased voltage. When the voltage doubler reaches a steady state, the transistors supplant the diodes in controlling the switching. With the transistors, there is a lower voltage drop along the branches of the bridge. The voltage drop is discussed on pages 4 and 5 of the specification, with regard to equations 1 and 2. The cited art does not teach or suggest the bridge as recited in claim 3. Although, as the office action indicates, there are bulk diodes in the transistors of Okada and Matsumura, Okada and Matsumura do not teach or suggest how those diodes are arranged. They are not arranged so that there are conduction paths parallel to the transistors or so that there is a lower voltage drop when the doubler reaches a steady state. In fact, given the arrangement of the transistors in Okada and Matsumura, they do not have bulk diodes which will conduct as recited in claim 3. Accordingly, claim 3 patentably distinguishes over the cited art and is in condition for allowance.

Claim 6 recites a voltage booster including an oscillator, a charge accumulation condensor and at least one charging section. Each of the at least one charging sections includes a first charge transfer condensor, a second charge transfer condensor, and a bridge of controlled switches. Neither Okada nor Matsumura teaches or suggests a voltage booster having at least one charging section formed of a bridge of controlled switches. Rather, in both Okada and Matsumura, two of the

transistors (TD1, TD2) and (13 and 14) operate as diodes by having their gates and drains connected together. In response to a similar argument in the prior amendment, the office action asserts that the limitation of having more than two controlled switches has never been claimed. Applicants respectfully assert that a "bridge", as recited in claim 6, is a known structure which includes four interconnected sides. Therefore, a bridge of controlled switches would necessarily include four switches. However, in order to further prosecution of this application, applicants have amended claim 6 to specifically recite a bridge of <u>four</u> controlled switches. Accordingly, claim 6 patentably distinguishes over the cited art.

Furthermore, claim 6 recites that the value of the voltage of the output corresponds to the continuous power voltage plus a product of the continuous power voltage and the number of the at least one charging section. One of the advantages of the present invention is that the output of the voltage multiplier is not effected by the threshold voltage of the transistors. In both Okada and Matsumura, the output is decreased by the threshold voltage. Therefore, the structures in Okada and Matsumura do not provide an output which has the value as recited in claim 6. Claim 6 patentably distinguishes over the cited art and this in condition for allowance.

Claims 7-11 depend from claim 6 and are allowable for at least the same reasons. Claim 7 further recites that the switches of the bridge are arranged to form two inverters connected in a loop to form a flip-flop. As discussed above with respect to claim 1, the structures in Okada and Matsumura do not include inverters which are arranged in a loop to form a flip-flop. Furthermore, applicants have amended claim 7, similar to claim 1, to recite two CMOS inverters. Thus, claim 7

further distinguishes over the cited art. Claim 9 recites that bulk terminals of the MOS transistors are connected in a way to create a one-way conduction path between the power input terminal and the charge output terminal when the switches are not conducting. Although applicants acknowledge that the transistors in Okada and Matsumura would have bulk diodes, those transistors are not arranged so that the bulk diodes provide a conduction path between the power input and output terminals when the switches are not conducting. If the switches are not conducting in Okada and Matsumura, no charge can pass. Thus, claim 9 further distinguishes over the cited art.

Independent claim 13 recites an electrically programmable non-volatile memory device including an oscillator, charge accumulation condensor, and at least one charging section. As with claim 6, the at least one charging section includes a first charge transfer condensor, a second charge transfer condensor, and a bridge of controlled switches. Also, the value of the voltage of the output is equal to the low voltage plus a product of the low voltage and the number of the at least one charging section. As discussed above with claim 6, the cited art does not teach or suggest the at least one charging section as recited in claim 13. Accordingly, claim 13 patentably distinguishes over the cited art.

Similarly, claim 14 recites a voltage regulator having a low voltage drop including an oscillator, a charge accumulation condensor, and at least one charging section. The at least one charging section includes the same elements as claims 6 and 13. Accordingly, claim 14 is allowable for at least the same reasons.

Independent claim 19 recites a voltage multiplier including an oscillator, a multiplying means

and an output means. The multiplying means includes at least one first charge transfer condensor, at least one second charge transfer condensor, and at least one bridge circuit of four controlled switches. Claim 19 is allowable for at least the same reasons as discussed above with respect to claims 6, 13, and 14. Claims 16-18 depend from claim 19 and are allowable for at least the same reasons.

Claims 20-22 also depend from claim 19. Claim 20 recites that the multiplying means includes a plurality of charge transfer condensors, and a plurality of bridge circuits. Neither Okada nor Matsumura teaches or suggests a plurality of bridge circuits. In response to applicants prior argument with regard to claims 20, 22, and 25 relating to the plurality of bridge circuits, the office action asserts that the rejection is a "combination rejection" which cannot be attacked by discussing the references individually. However, claims 20, 22 and 25 were not rejected over a combination of references. Rather, they were separately rejected as being obvious extensions of the principal references, Matsumura or Okada. Applicant has not simply argued that Matsumura and Okada do not <u>disclose</u> multiple bridge circuits. Rather, applicants have argued that Okada and Matsumura fail to teach or suggest anything regarding multiple bridge circuits. Without any teaching or suggestion, it would not be obvious to one skilled in the art to do so. Therefore, claims 20-22 distinguish over the cited art.

The office action then asserts that it is "notoriously well-known" to use multiple stages of charge pumps in series to obtain different output magnitudes. However, Asari, the only reference referred to in the office action (but not relied upon in the rejection), is not combinable with Okada

or Matsumura. Asari teaches a voltage step-up circuit having a first series of an odd number of inverters in a second series of an even number of inverters. The output from the series of inverters are applied to condensors connected to the gates of series connected transistors. The output of the series of transistors provides the stepped-up voltage. There is nothing in Asari which teaches or suggests a bridge circuit or how the bridge circuit in Okada or Matsumura would be included in conjunction with the inverters or transistors of the structure of Asari. Accordingly, Asari cannot be combined with the cited art, and claims 20 and 22 patentably distinguish over the cited art.

Claim 24 recites a method for generating an output voltage including the steps of generating a first and second periodic signals, applying these signals to first and second charge transfer condensors and generating an output based upon the input voltage and the first and second charge transfer condensors. The step of generating the output includes applying the voltages to a bridge circuit and applying the output of the bridge circuit to a charge accumulation condensor. The bridge circuit includes four controlled switches. As discussed above with claim 6, the cited art does not teach or suggest bridge circuits having four controlled switches. Accordingly, claim 24 patentably distinguishes over the cited art.

Claim 25 also recites the method for generating a principal output voltage. It is similar to claim 24 and recites applying the signals to a plurality of first and second charge transfer condensors and in applying the outputs of the charge transfer condensors to a plurality of bridge circuits, each including four controlled switches. Claim 25 distinguishes over the cited art for at least the same reasons as claim 24. Furthermore, as discussed above with claim 20, the cited art does not teach or

suggest the use of a plurality of bridge circuits. Accordingly, claim 25 patentably distinguishes over the cited art and is in condition for allowance.

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

Francesco Pulvirenti and Roberto Gariboldi

By Brett N Dorny

Brett N. Dorny, Reg. No. 35,860
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, MA 02210-2211
Attorneys for Applicant(s)
Tel. no. (617) 720-3500